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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/585,864	06/01/2000	Wen Li	4309US ( 99-1328 )	4732

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Joseph A Walkowski  
Trask Britt  
P O Box 2550  
Salt Lake City, UT 84110

EXAMINER

BURD, KEVIN MICHAEL

ART UNIT	PAPER NUMBER
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2631

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DATE MAILED: 03/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/585,864

Applicant(s)

LI ET AL.

Examiner

Kevin M Burd

Art Unit

2631

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 27 November 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 November 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 2.
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_.

***Information Disclosure Statement***

1. The information disclosure statement (IDS) submitted on 6/1/2000 is being considered by the examiner.

***Drawings***

2. The drawings are objected to because the elements of figure 6 need to contain a text label as well as a numerical label. An example is element 216 on figure 6, which should be labeled silicon wafer. It is office policy to request from Applicants that submitted figure contain both of the above stated labels to allow individuals viewing each figure to be able to determine the elements in the figure without having to go into the specifications to determine what the designation of each element in a figure. This is simply a request and this objection to the figures will be withdrawn in the next office action.

***Specification***

3. The abstract of the disclosure is objected to because line 15 should be deleted. Correction is required. See MPEP § 608.01(b).

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Saitoh et al (US 5,604,775).

Regarding claims 1, 8-10 and 12-16, Saitoh discloses a method of adjusting a reference clock as shown in figure <sup>3A</sup>~~3~~. A reference clock (local clock) is input to the coarse stepsize delay 11 and the signal is delayed according to the control signal from latch 43. This delayed signal (first delayed signal) is input to the fine step size delay 12 and delayed according to the control signal input from latch 43. The fine delay outputs a delayed signal (second delayed signal). A feedback signal is output from the delay circuits and feed to the phase detector 30 to provide a timing signal. This timing signal is used to form the control signal to adjust the delay lines shown in figure 3.

Regarding claims 2-4, the timing signal is a result of the reference clock being delayed through the coarse and fine delays. Since the feedback signal is generated from the outputs of the delay circuits, the rising and falling edges of the timing signal will be generated according to the outputs of the delay circuit.

Regarding claim 5, phase detector 30 compares the inputs of the reference clock and the timing signal to generate the control signals to adjust the delays of the coarse and fine delay elements as shown in figure 3.

Regarding claims 6 and 7, when the output of the phase detector is zero, no delay adjustment is needed.

Regarding claim 11, figure 6 discloses generating an inverse clock signal in the fine delay since the delay comprises a plurality of inverters. The timing signal is generated from these delays.

5. Claims 17-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Richley (US 5,223,755).

Regarding claims 17, 23 and 24, Richley discloses a data synchronizing circuit in figure 1. Phase detectors 22 and 26 compare the phases of the output of the delay elements 20 and 12 and the input clock. A control signal is input to delay line 20.

Regarding claim 18, element 20 is a delay line and delay lines comprise a plurality of delay elements. This delay line receives a clock input and a control signal to vary the delay value of the delay line. The delay line is coupled to the phase detectors as shown in figure 1.

Regarding claim 19, the circuitry is coupled to the output of the delay line and is responsive to the rising and falling of the delayed signal.

Regarding claims 20 and 21, element 20 is a delay line and delay lines comprise a plurality of delay elements.

Regarding claim 22, inverters are routinely used in delay lines to delay signals. This fact is shown in figure 1, elements 12 and 40 are delay circuits comprised of inverters.

**Contact Information**

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks  
Washington, D.C. 20231

**or faxed to:**

(703) 872-9314, (for formal communications intended for entry or for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Burd, whose telephone number is (703) 308-7034. The Examiner can normally be reached on Monday-Thursday from 9:00 AM - 6:00 PM.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3800.



Kevin M. Burd  
PATENT EXAMINER  
3/9/2004